DM13A

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16-bit Constant Current LED Driver

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DM13A

16-bit Constant Current LED Driver

General Description

DM13A is a constant-current sink driver specifically designed for LED display applications. The device incorporates shift registers, data latches, and constant current circuitry on the silicon CMOS chip. The maximum output current value of all 16 channels is adjustable by a single external resistor.

Features

- Constant-current outputs: 3mA to 60mA adjustable by one external resistor
- Maximum output voltage: 17V
- Maximum clock frequency: 25MHz
- Power supply voltage: 3.3V to 5V
- In-rush current control
- Bit-to-bit skew : ± 3 % Chip-to-chip skew : ± 6 %
- Package and pin assignment compatible to conventional LED drivers (ST2221C, DM134/5/6)

Applications

- Indoor/Outdoor LED Video Display
- LED Variable Message Signs (VMS) System

Package Types

- PDIP24, SOP24, SOP24B, SSOP24

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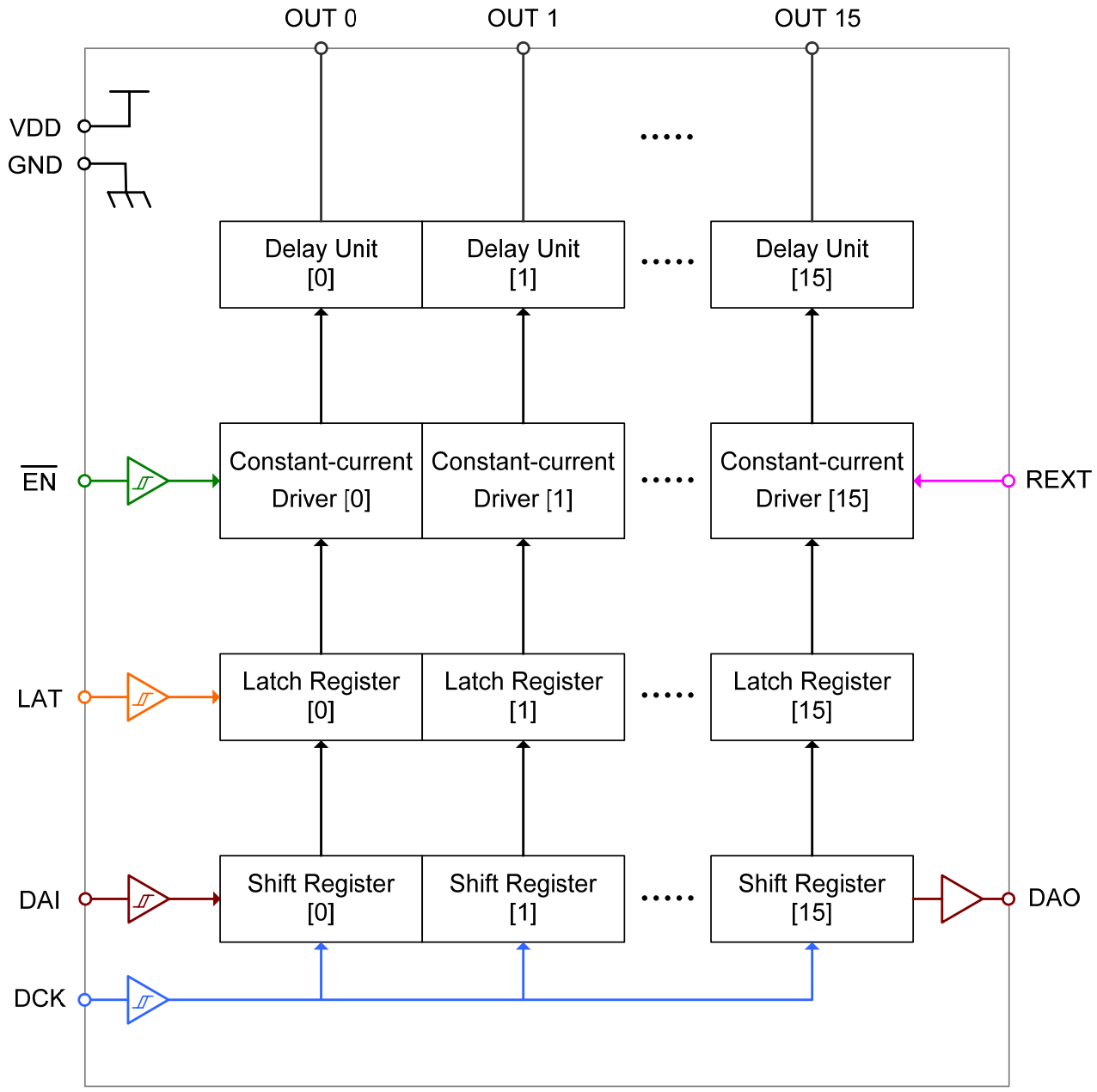
Block Diagram



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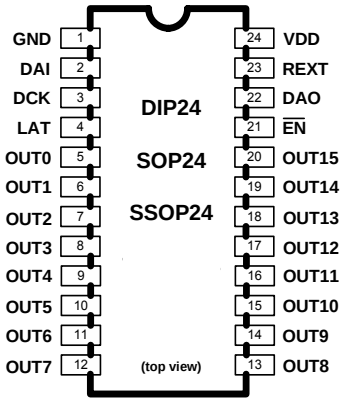
Pin Connection



Pin Description

PIN No.	PIN NAME	FUNCTION
DIP24/SOP24/SSOP24: 1	GND	Ground terminal.
DIP24/SOP24/SSOP24: 2	DAI	Serial data input terminal.
DIP24/SOP24/SSOP24: 3	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
DIP24/SOP24/SSOP24: 4	LAT	Input terminal of data strobe. Data on shift register goes through at the high level of LAT (level trigger). Otherwise, data is latched.
DIP24/SOP24/SSOP24: 5~20	OUT0~15	Sink constant-current outputs (open-drain).
DIP24/SOP24/SSOP24: 21	$\overline{EN}$	Output enable terminal: **'H'** for all outputs are turned off , **'L'** for all outputs are active.
DIP24/SOP24/SSOP24: 22	DAO	Serial data output terminal.
DIP24/SOP24/SSOP24: 23	REXT	External resistors connected between REXT and GND for output current value setting.
DIP24/SOP24/SSOP24: 24	VDD	Supply voltage terminal.

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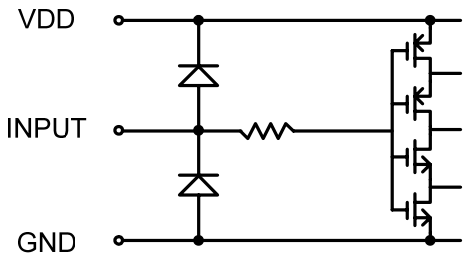
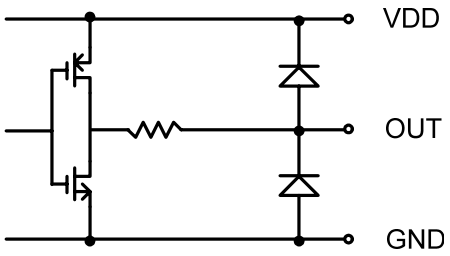
Equivalent Circuit of Inputs and Outputs

1. DCK, DAI, LAT, $\overline{EN}$ terminals



2. DAO terminals



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Maximum Ratings[*1] (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	70	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	25	MHz
GND Terminal Current	IGND	1500	mA
Power Dissipation (4 layer PCB)	PD	1.90 (PDIP24 : Ta=25°C)	W
		1.20 (SOP24 : Ta=25°C)	
		TBD(SOP24B : Ta=25°C)	
		1.05 (SSOP24 : Ta=25°C)	
Thermal Resistance	Rth(j-a)	50.0 (PDIP24)	°C/W
		TBD (SOP24B)	
		79.2 (SOP24)	
		90.2 (SSOP24)	
Operating Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	—	3.3	5.0	5.5	V
Output Voltage	VOUT	Driver On[*2]	1.0	—	0.5VDD	V
Output Voltage	VOUT	Driver Off[*3]	—	—	17	
Output Current	IO	OUTn	5	—	60	mA
	IOH	VOH = VDD – 0.2 V	—	—	+1.2	
	IOL	VOL = 0.2 V	—	—	−1.4	
Input Voltage	VIH	VDD = 3.3 V ~ 5.5V	0.8VDD	—	VDD	V
	VIL		0.0	—	0.2VDD	
Input Clock Frequency	FDCK	Single Chip Operation	—	—	25	MHz
LAT Pulse Width	tw LAT	VDD = 5.0V	15	—	—	ns
DCK Pulse Width	tw DCK		15	—	—	
Set-up Time for DAI	tsetup(D)		10	—	—	
Hold Time for DAI	thold(D)		10	—	—	
Set-up Time for LAT	tsetup(L)		10	—	—	
Hold Time for LAT	thold(L)		10	—	—	

[*1] Stress beyond those listed under “Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; it’s not implied functional operation condition. Exposure to “Maximum Ratings” conditions for extended periods may affect device reliability and life time.
[*2] Notice that the power dissipation is limited to its package and ambient temperature.
[*3] The driver output voltage including any overshoot stress has to be compliant with the maximum voltage (17V).

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Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.8VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logics2 level	GND	—	0.2VDD	
Output Leakage Current	IOL	VOH = 17 V	—	—	±1.0	uA
Output Voltage (DAO)	VOL	IOL = 1.5 mA	—	—	0.2	V
	VOH	IOH= 1.4 mA	VDD-0.2	—	—	
Output Current Skew (Channel-to-Channel) *1	IOL1	VOUT = 1.0 V Rrext = 2.2KΩ	—	—	±3	%
Output Current Skew (Chip-to-Chip) *2	IOL2		—	—	±6	%
Output Voltage Regulation	% / VOUT	Rrext = 2.2KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VDD	Rrext = 2.2 KΩ	—	±1	±4	
Supply Current *3	$I_{DD(off)}$	power on all pins are open unless VDD and GND	—	3	4	mA
	$I_{DD(off)}$	input signal is static Rrext = 2.9 KΩ all outputs turn off	—	5	6	
	$I_{DD(on)}$	input signal is static Rrext = 2.9 KΩ all outputs turn on	—	5	6	
	$I_{DD(off)}$	input signal is static Rrext = 1.05K Ω all outputs turn off	—	9	10	
	$I_{DD(on)}$	input signal is static Rrext = 1.05K Ω all outputs turn on	—	9	10	

*1 Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.
*2 Chip-to-Chip skew is defined as the range into which any output current of any IC falls.
*3 IO excluded.

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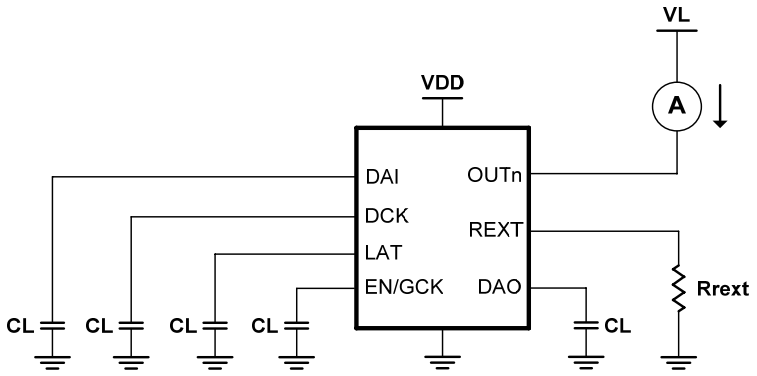
Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	EN-to-OUT0	tpLH	VIH = VDD VIL = GND Rrext = 2.2KΩ VL = 5.0 V CL*1 = 13 pF	—	52	—	ns
	LAT-to-OUT0			—	49	—	
	DCK-to-DAO			—	20	—	
Propagation Delay ('H' to 'L')	EN-to-OUT0	tpHL		—	22	—	
	LAT-to-OUT0			—	75	—	
	DCK-to-DAO			—	19.5	—	
Output Current Rise Time		tor		—	33.5	—	
Output Current Fall Time		tof		—	6	—	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+1)}$)		tod		—	5	—	

Switching Characteristics (VDD = 3.3V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L' to 'H')	EN-to-OUT0	tpLH	VIH = VDD VIL = GND Rrext = 2.2KΩ VL = 5.0 V CL*1 = 13 pF	—	51	—	ns
	LAT-to-OUT0			—	21.5	—	
	DCK-to-DAO			—	12	—	
Propagation Delay ('H' to 'L')	EN-to-OUT0	tpHL		—	23	—	
	LAT-to-OUT0			—	49	—	
	DCK-to-DAO			—	11.5	—	
Output Current Rise Time		tor		—	35	—	
Output Current Fall Time		tof		—	10	—	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+1)}$)		tod		—	10	—	



Switching Characteristics Test Circuit

*1 CL means the probe capacitance of oscilloscope.

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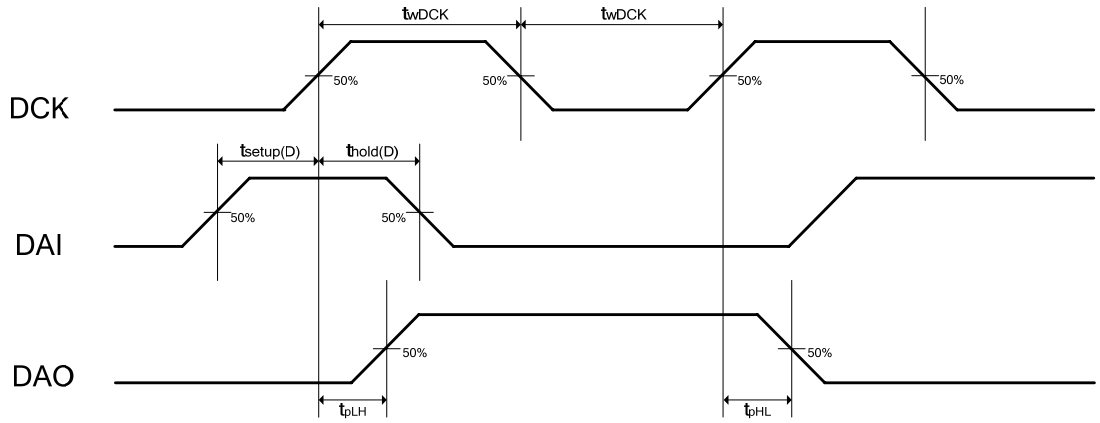
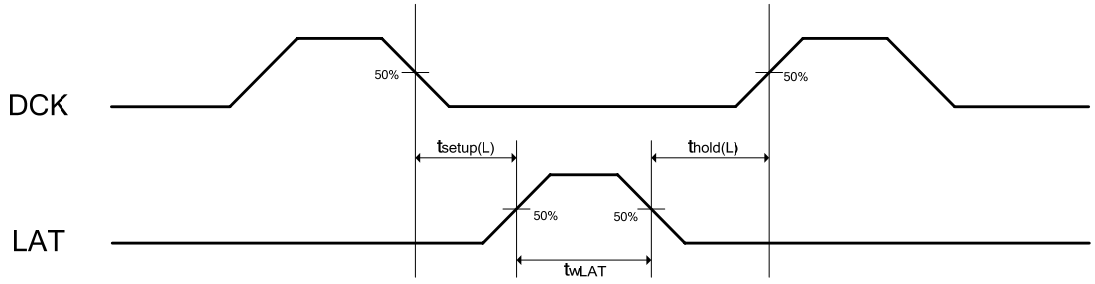
Timing Diagram

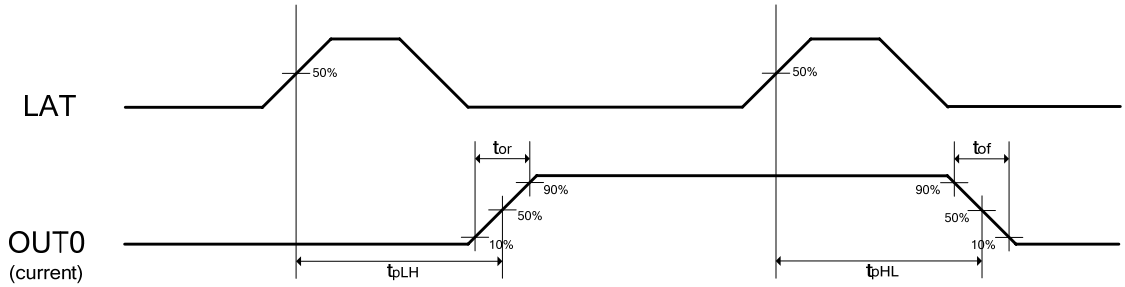
1. DCK-DAI, DAO



2. DCK-LAT



3. LAT-OUT0



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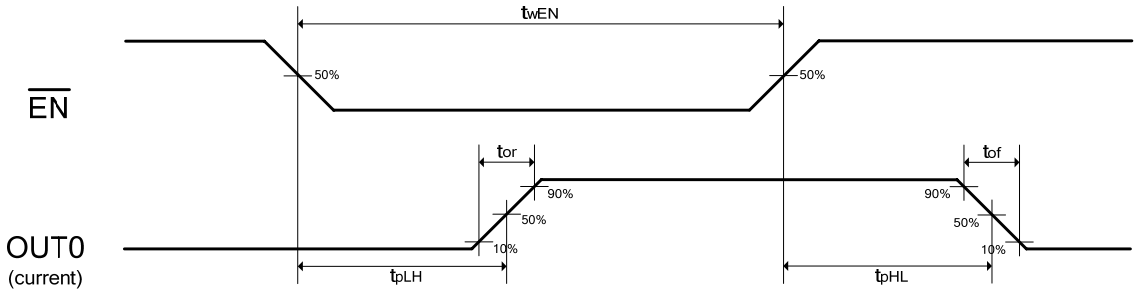
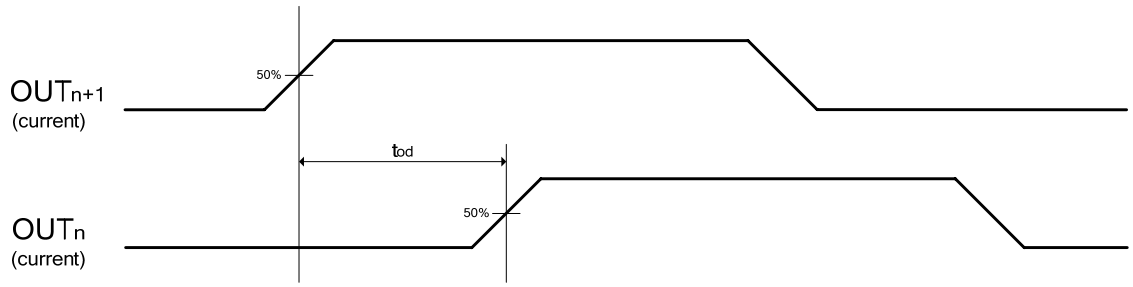
4. $\overline{EN}$-OUT0



5. OUT_{n+1}-OUT_n



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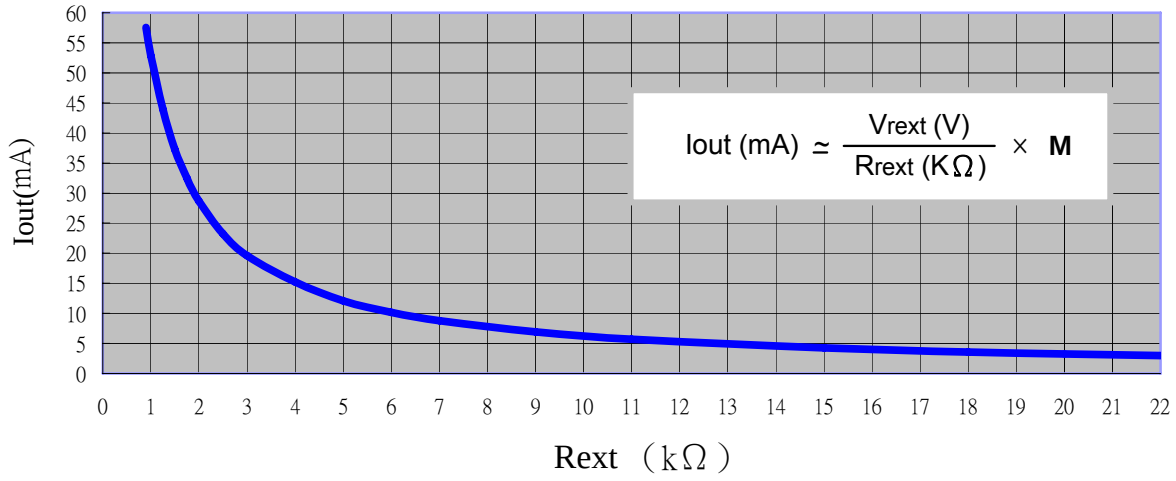
Constant-Current Output

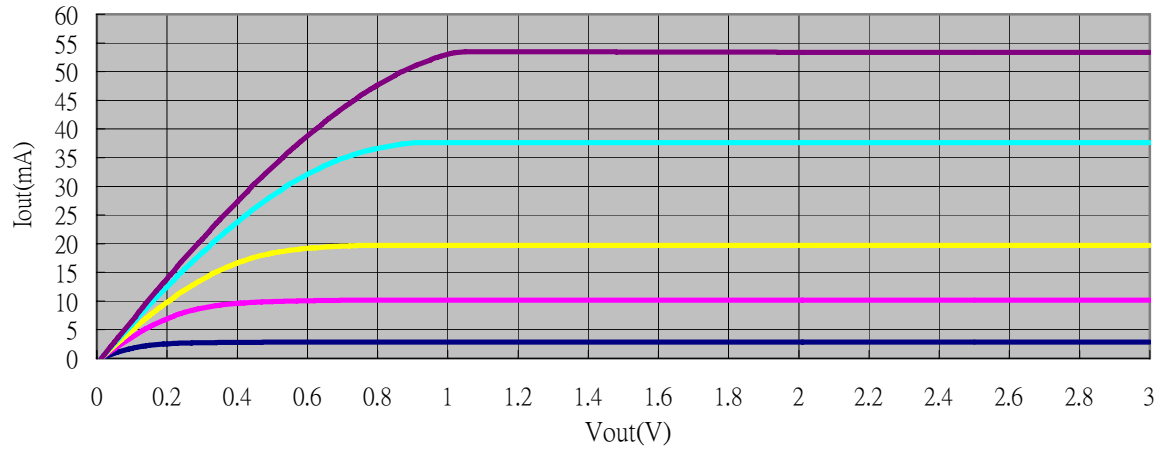
Constant-current value of each output channel is set by an external resistor connected between the REXT pin and GND. Varying the resistor value can adjust the current scale ranging from 3mA to 60mA. The reference voltage of REXT terminal (Vrext) is approximately 1.2V. The output current value is calculated roughly by the following equation:

Iout(mA)	3	5	10	20	30	40	50
M	55	54.1	50	46.6	45	43.3	41.6

Output Current as a Function of Rrext value



Output Current as a Function of Output Voltage



In order to obtain a good performance of constant-current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage above.

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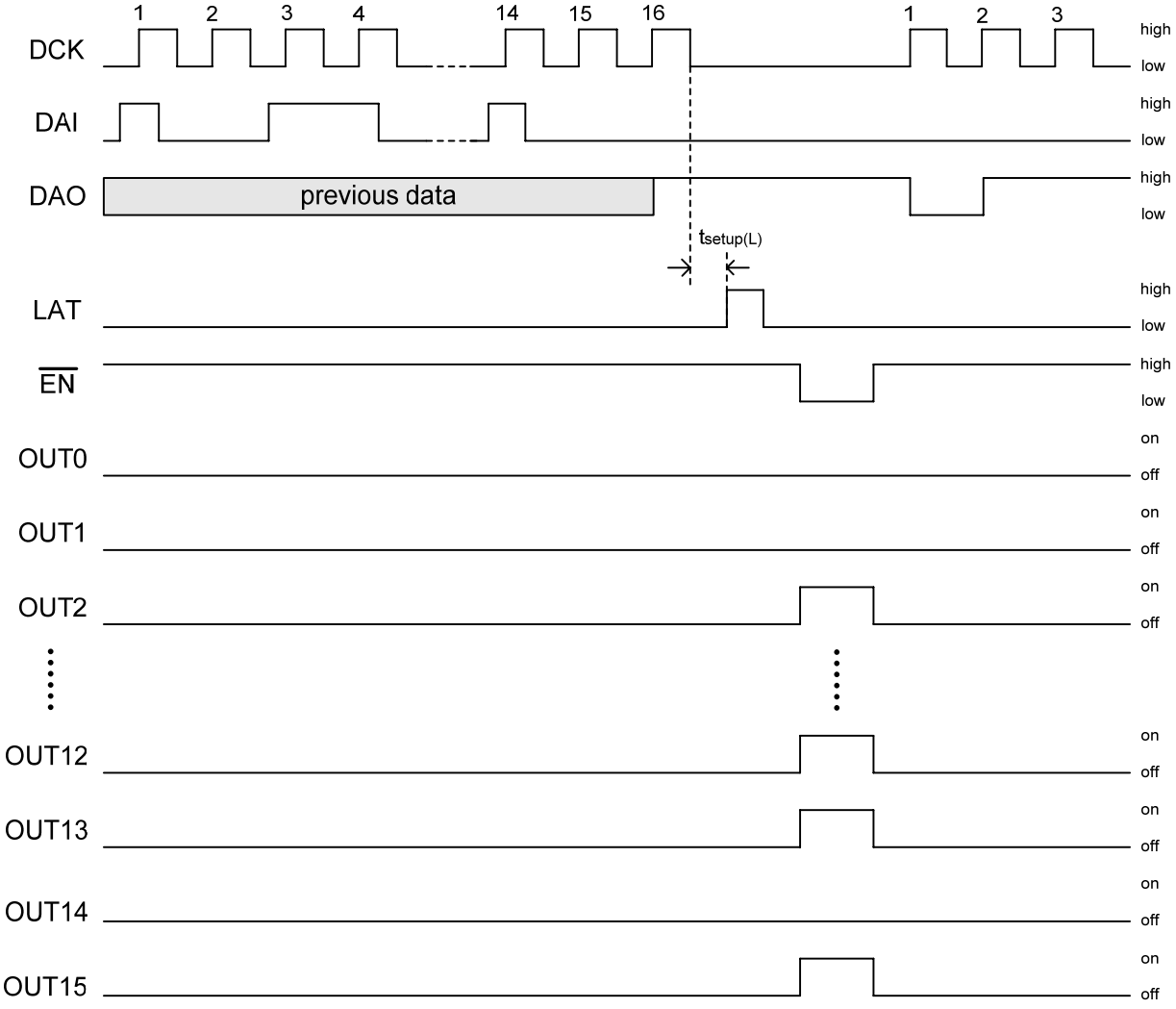
Serial Data Interface

The serial-in data (DAI) will be clocked into 16 bit shift register synchronized on the rising edge of the clock (DCK). The data ‘1’ represents the corresponding current output ‘ON’, while the data ‘0’ stands for ‘OFF’. The data will be transferred into the 16 bit latch register when the strobe signal (LAT) is ‘H’ (level trigger); otherwise, the data will be held. The trigger timing of the serial-out data (DAO) will be shifted out on synchronization to the rising edge of the clock. All outputs are turned off while enable terminal (EN) is kept at high level. And they are active when EN shifts to low.



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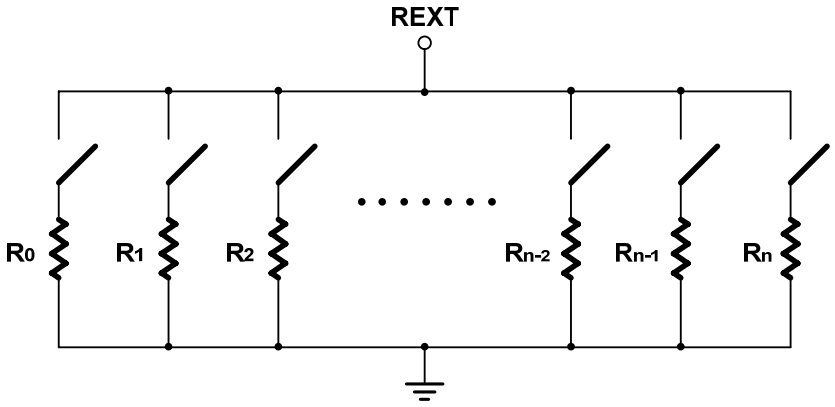
Outputs Delay

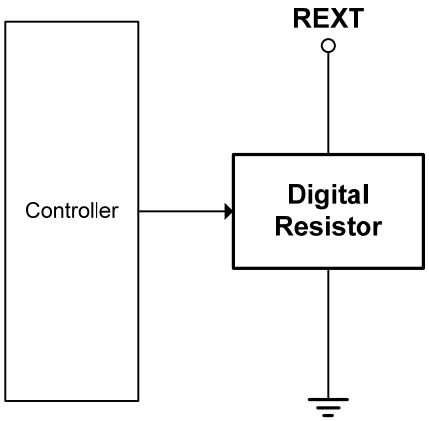
Large in-rush currents will occur when the system activates all the outputs at once. To reduce this effect, DM13A is designed to have a constant unit of delay (around 5ns) between outputs. The delay sequence for every output goes like this: OUT0 (no delay) → OUT15 → OUT1 → OUT14 → OUT2 → OUT13 → OUT3 → OUT12 → OUT4 → OUT11 → OUT5 → OUT10 → OUT6 → OUT9 → OUT7 → OUT8 (the largest delay).

Global Brightness Control

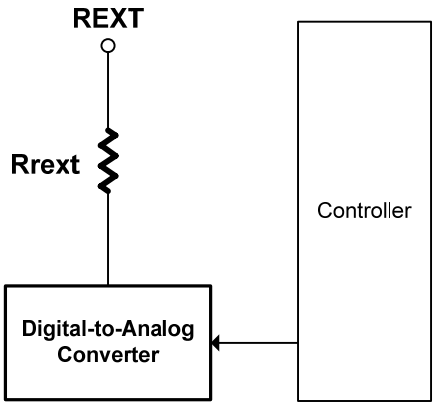
DM13A has no built-in global brightness control feature. In order to obtain a lower resolution of global brightness control effect, two methods could be utilized. One is providing PWM signal synchronized on latch pulse to modulate the output enable terminal ($\overline{EN}$ pin). The other is to adjust the Rrext value or voltage drop across the external resistor. Please see the reference circuit below:



Global Brightness Control with Resistor Ladder



Global Brightness Control
with Digital Resistor



Global Brightness Control
with D/A converter

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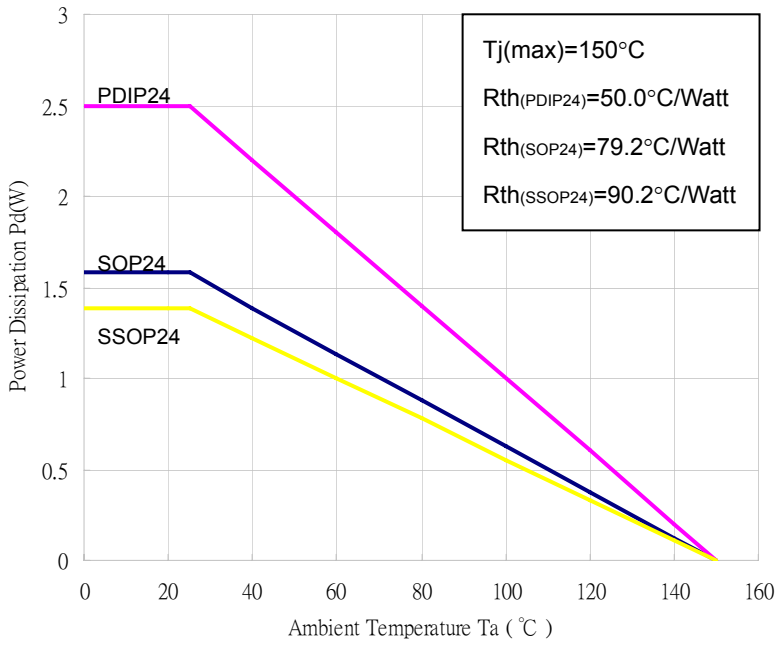
Power Dissipation

The power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(℃) - Ta(ambient\ temperature)(℃)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(℃/Watt)}$$

The relationship between power dissipation and operating temperature can be refer to the figure below:



The power consumption of IC can be determined by the following equation and should be less than the maximum allowable power dissipation:

$$Pd(W) = V_{CC}(V) \times I_{DD}(A) + Vout0 \times Iout0 \times Duty0 + \cdots\cdots + Vout15 \times Iout15 \times Duty15 \leq Pd(max)(W)$$

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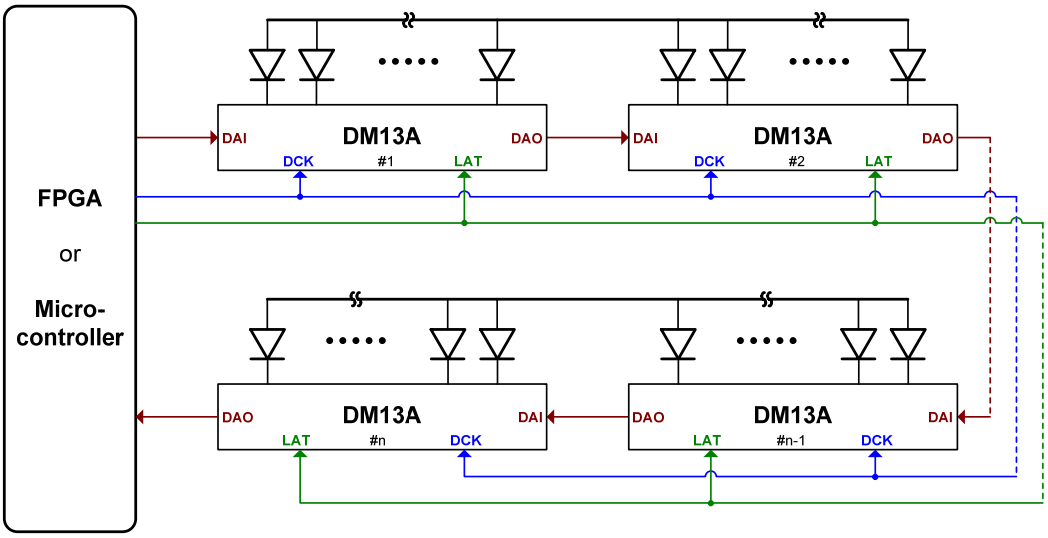
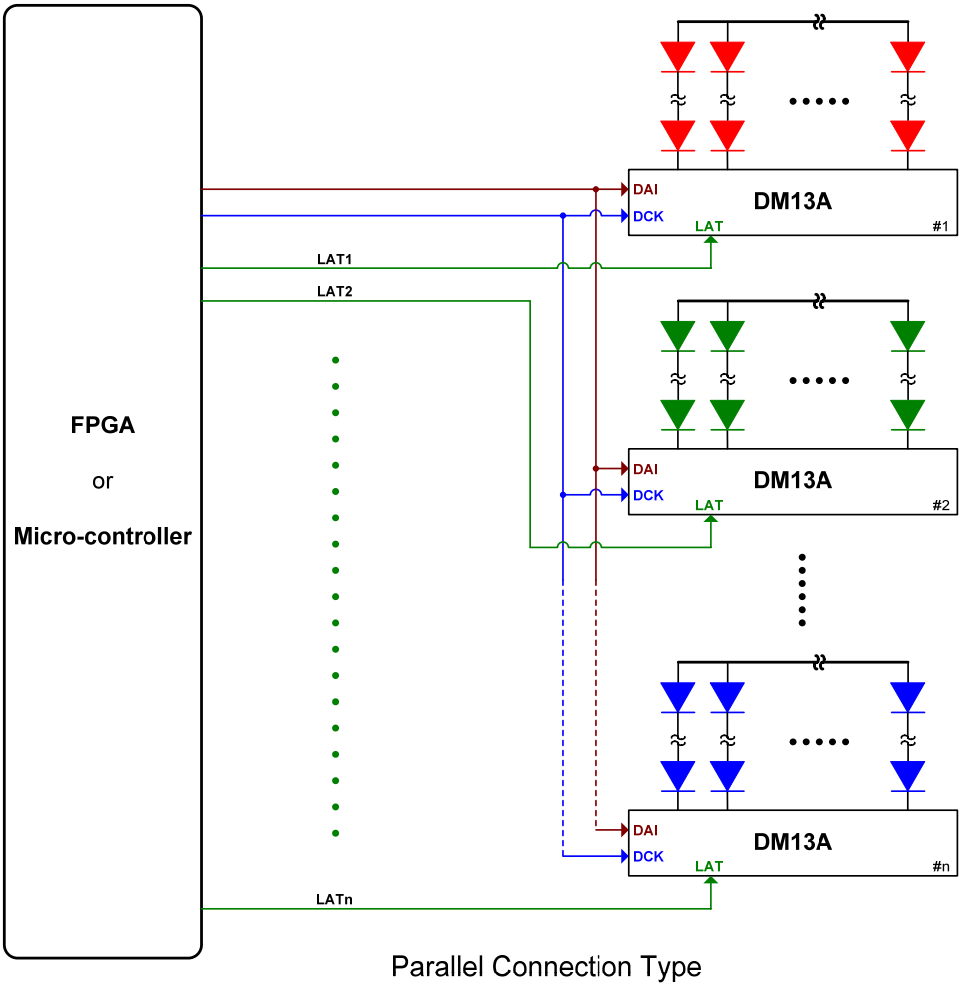
Typical Application



Serial Connection Type



Parallel Connection Type

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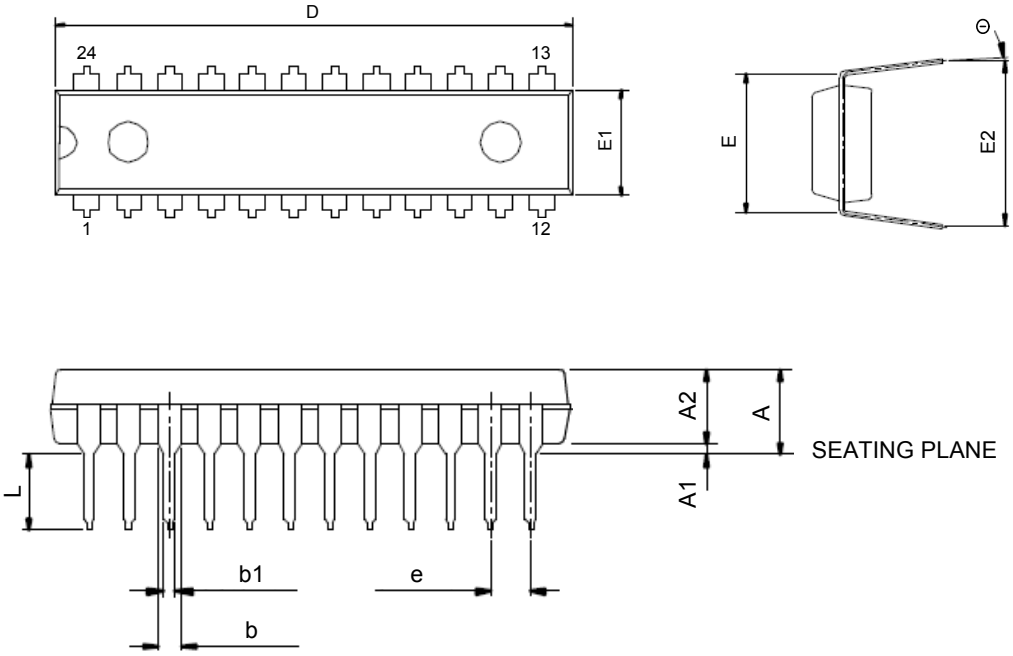
Package Outline Dimension

PDIP24



	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	0.210	-	5.334
A1	0.015	-	0.381	-
A2	0.125	0.135	3.175	3.429
b	0.060TYP.		1.524TYP.	
b1	0.018TYP.		0.457TYP.	
D	1.230	1.280	31.242	32.521
E	0.300TYP.		7.620TYP.	
E1	0.253	0.263	6.426	6.680
E2	0.335	0.375-	8.509	9.525
e	0.100TYP.		2.540TYP.	
L	0.115	0.150	2.921	3.810
Θ	0°	15°	0°	15°

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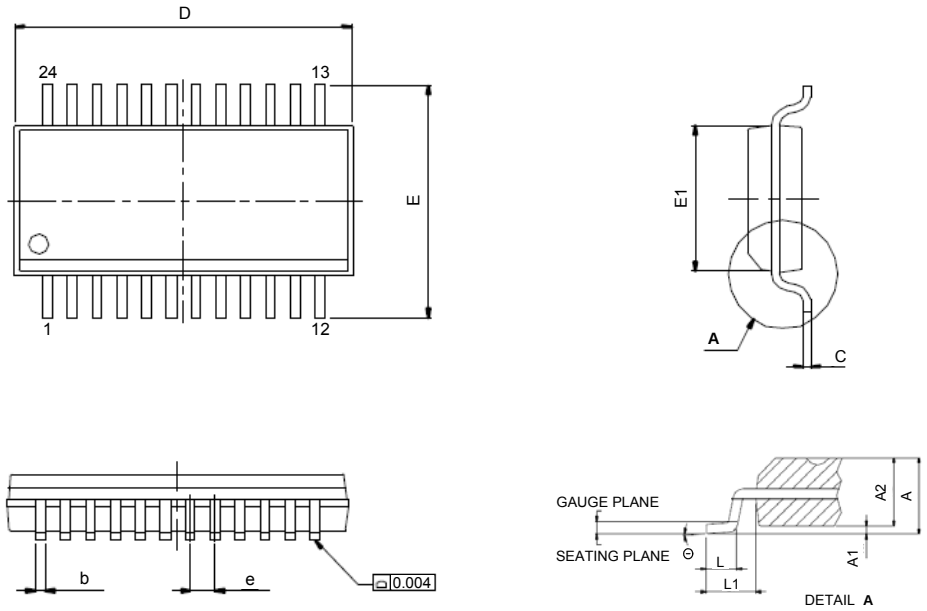
Package Outline Dimension

SSOP24



	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.346	1.753
A1	0.004	0.010	0.102	0.254
A2	-	0.059	-	1.499
b	0.008	0.012	0.203	0.305
C	0.007	0.010	0.178	0.254
D	0.337	0.344	8.560	8.738
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
e	0.025TYP.		0.635TYP.	
L	0.016	0.050	0.406	1.270
L1	0.041TYP.		1.041TYP.	
Θ	0°	8°	0°	8°

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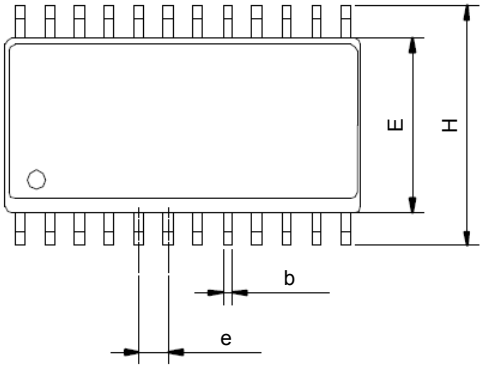
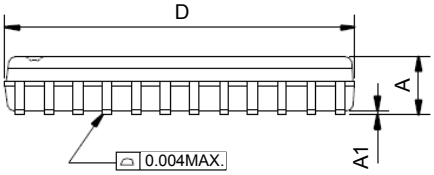
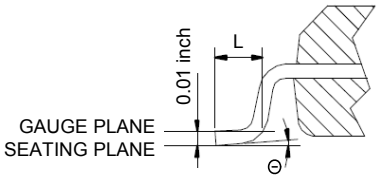
Package Outline Dimension

SOP24







	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	0.093	0.104	2.362	2.642
A1	0.004	0.012	0.102	0.305
b	0.016TYP.		0.406TYP.	
D	0.599	0.614	15.215	15.596
E	0.291	0.299	7.391	7.595
e	0.050TYP.		1.270TYP.	
H	0.394	0.419	10.008	10.643
L	0.016	0.050	0.406	1.270
Θ	0°	8°	0°	8°

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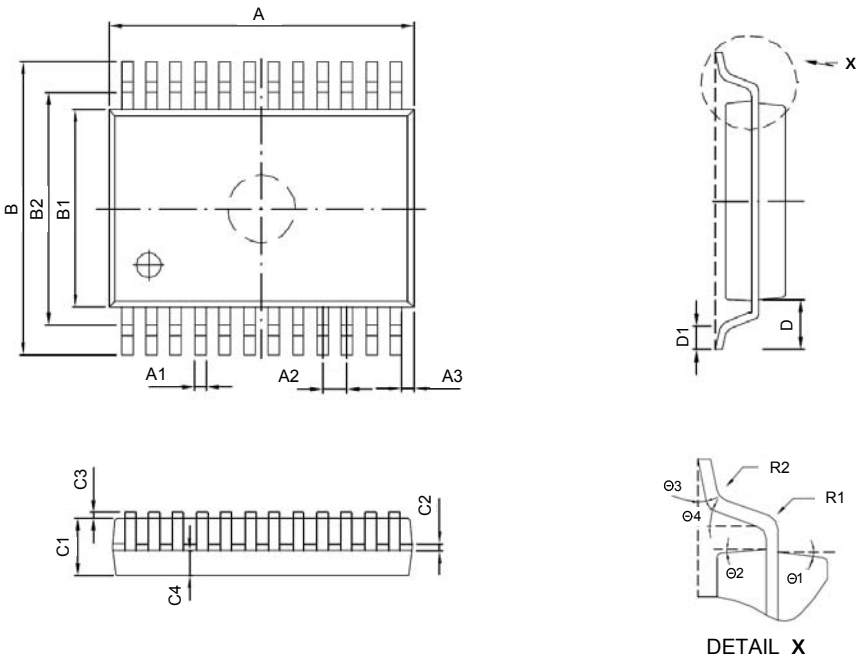
Package Outline Dimension

SOP24B



	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	0.508	0.516	12.9	13.1
A1	0.012	0.020	0.30	0.50
A2	0.039TYP.		1.00TYP.	
A3	0.031		0.80TYP.	
B	0.299	0.323	7.60	8.20
B1	0.232	0.240	5.90	6.10
B2	0.300TYP.		7.62TYP.	
C	-	0.087	-	2.20
C1	0.067	0.075	1.70	1.90
C2	0.006	0.012	0.15	0.30
C3	0.002	0.008	0.05	0.20
C4	0.031TYP.		0.80TYP.	
D	0.037TYP.		0.95TYP.	
D1	0.013	0.029	0.33	0.73
R1	0.008TYP.		0.20TYP.	
R2	0.008TYP.		0.20TYP.	
Θ1	8°TYP		8°TYP	
Θ2	10°TYP		10°TYP	
Θ3	4°TYP		4°TYP	
Θ4	5°TYP		5°TYP	

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